Remarks and Arguments in Favor of Patentability

I. Claim Rejections Under 35 U.S.C. § 112

In paragraph 3 of the Office Action, the Examiner rejects claims 8, 10, 11, 16, 19, 20, and 21 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The Examiner asserts that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

In reference to claims 8 and 16, wherein "said second layer is oxide" is not disclosed or described in the specification: claims 8 and 16 now read in part "… wherein said first layer and said second layer are polysilicon" to correlate with the specification.

In reference to claims 10 and 19, wherein said substrate layer further comprises "a thin surface layer" is not disclosed or described in the specification: claims 10 and 19 have been canceled.

In reference to claims 11, 20, and 21 which are rejected for not disclosing "an input/output port in communication with said memory array" and/or "a controller coupled to said input/output port and said memory array" is not disclosed or described in the specification: a new paragraph, provided supra, is to be inserted in the specification section of the application at page 7, line 33 and a new Fig. 3B added to illustrate the input/output port description. This new paragraph includes "an input/output port in communication …" and "a controller …"

Therefore, Applicant submits that in light of the above amendments, claims 8, 10, 11, 16, 19, 20, and

21 claim, with sufficient particularity to be patentable, the subject matter which Applicant regards as the invention. The Applicant also submits that the claims are being amended solely for the purpose of placing them in better form and not to overcome any existing or potential prior art issues.

II. Claim Rejections Under 35 U.S.C. § 102(b)

In paragraph 9 of the Office Action, the Examiner rejects claims 5-7 and 13-15 under 35 U.S.C. § 102(b). Independent claims 5 and 13 have been amended to more fully differentiate the claimed invention from the prior art.

For instance, claim 5 is amended to read "a buried implant region essentially contiguous with said source implant region, a tunnel diode window region within said buried implant region" (lines 3-6), "a floating gate oxide layer overlaying said floating gate transistor region exclusive of said tunnel diode window region" (lines 11-13), and "an interpoly layer overlaying said first layer and said active region, said interpoly layer extending essentially continuous from an edge of said source implant region to an edge of said drain implant region " (lines 16-19). Claim 13 is similarly amended with regard to doped regions.

The Examiner cites the U.S. Patent No. 6,420,753 (hereinafter "the '753 patent"), wherein "[a] first insulating layer, including regions 114, 146, and 148, is generally deposited over the substrate 130" (column 8, lines 36-37). In the claimed invention "a tunnel oxide layer overlaying a portion of said buried implant region" (claim 5, lines 9-10) along with the floating gate oxide layer, described supra (claim 5, lines 9-13), form a two layered implementation of the oxide formation beneath the floating gate, thus distinguishing it from the '753 patent. This claimed

element is supported and clearly distinguishable in amended Fig. 4B, by the elements gate ONO layer 450 and tunnel oxide 460 layer.

The '753 patent further describes formation of the control and select devices as "[a] control gate 138 is disposed over the second insulating layer and extension a portion of the floating gate 140. A select transistor is disposed over the second insulating layer as well. In fact, in this memory cell embodiment, a select transistor is formed in series with a storage transistor 152." (column 8, lines 22-26). Note that **two devices** are portrayed as being in series in both Fig. 4c and the associated description of the '753 patent.

In contrast, control and select functions of the claimed invention are a **single device** represented as "a second layer extending continuously over said floating gate transistor region and said active region, said second layer extending from an edge of said source implant region to an edge of said drain implant region" (claim 5, lines 20-23). Therefore, the control and select structure of the claimed invention is clearly distinguishable over the plurality of devices of the '753 patent.

The '753 patent describes three distinct and completely separate diffused regions. Text of the '753 patent cited by the Examiner is described as "[r]eferring to FIG. 4c … in a like fashion, there are three regions, 132, 134, and 136, diffused into a substrate 130" (column 8, lines 13-16). The phrase "like fashion" is "[r]eferring to FIG. 4a, … [d]eposited on the substrate 100 are a drain region at 102 (or 104), a source region 104 (or 102), and a middle region 106 that forms a drain/source with respect to the respective source/drain region" (column 6, lines 55-63).

In contrast, the claimed invention, while also containing three diffusion regions, describes a **single**

source and drain diffusion with a high concentration buried diffusion in contact with the source (i.e., "a source implant region, a buried implant region contiguous with said source implant region, ... and a drain implant region," claim 5, lines 4-8). Claim 13 is similarly constructed and is therefore equally distinguishable from the '753 patent. The electrical structure of these diffusions of the claimed invention constitutes a single device.

Further, since the dependent claims 6, 7, 14, and 15 directly depend on either independent base claim 5 or 13 and consequently incorporate all limitations of claims 5 and 13, dependent claims 6, 7, 14, and 15 are therefore also distinguished from the '753 patent for at least the same reasons as independent base claims 5 and 13.

Based on the discussion, supra, the memory cell of the claimed invention has been shown to be patently distinct over the cited art. The Applicant therefore respectfully requests that the Examiner withdraw his claim rejections under 35 U.S.C. § 102(b) and allow claims 5-7 and 13-15.

III. Claim Rejections Under 35 U.S.C. § 103(a)

In paragraph 14 of the Office Action, the Examiner rejects claims 9, 12, 17, and 18 under 35 U.S.C. § 103(a), as being unpatentable over the '753 patent, in view of U.S. Patent No. 5,811,852 (hereinafter "the '852 patent"). The Examiner maintains that the '753 patent discloses the claim limitations of claims 5 and 13 except for the teachings of an ONO layer under the '852 patent. Amended base claims 5 and 13 have been shown to be patentably distinct over the cited art. Therefore, since claims 9, 12, 17, and 18 all depend from one of these two base claims, they too are allowable for at least the same reasons. In view of the above discussion, Applicant

requests that the 35 U.S.C. § 103 rejection be withdrawn from dependent claims 9, 12, 17, and 18, and that claims 9, 12, 17, and 18 be allowed.

IV. Conclusion

Therefore, in light of the amended claims, specification, and figures, Applicant contends that the claimed invention is in condition for allowance and earnestly solicits such a response. No new matter has been added by means of the specification or claim amendments or drawing substitutions. Changes made to the specification and drawings were merely to correct grammatical and typographical errors, as well as to clarify or correct reference numbers between the specification and the figures. All amendments and changes have been made only to more clearly point out what Applicant believes is his invention.

If the Examiner has any questions, he is invited to contact Applicant's representative at the number shown below.

CERTIFICATE OF MAILING

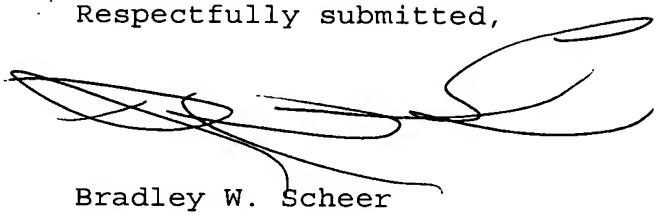
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313.

Signed: Sally Azevedo

Typed Name: Sally Azevedo

Date: August 27, 2004

Respectfully submitted,



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Amendments to the Drawings:

Applicant is amending Fig. 4B by adding and/or relocating labels for clarification and closer correspondence to Fig. 5G. Additions and changes are shown in red on the attached copy of Fig. 4B. Each label noted in red is either a relocation and/or copy of a previously used label or is used in paragraphs explaining these figures in the specification.

The label for gate ONO layer 450 is moved to better correlate with corresponding initial gate oxide layer 517 of Fig. 5E. The active region 414 is shown with a brace to better delineate its range. The interpoly layer 412 is now labeled at each extent between source implant region 406 and drain implant region 402. A line of delineation has been added between the gate ONO layer 450 and the inter poly layer 412 at the end of the floating gate 410, closest to the drain implant region 402, which extends down to the substrate surface. This matches with the previous representation of the corresponding interpoly dielectric layer 521 in Fig. 5G. Applicant avers that no new matter has been added as a result of the aforementioned changes.

Applicant is adding Fig. 3B to accompany a new paragraph inserted at page 7, line 33. This new figure includes an input/output port and a controller.

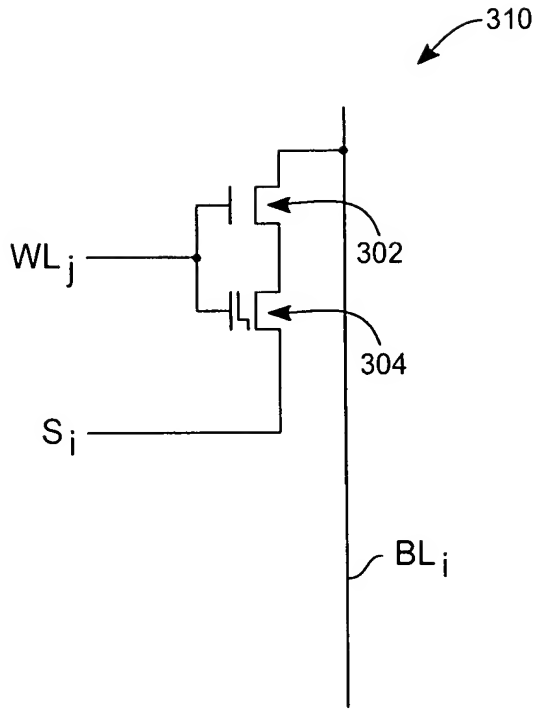

Fig. 4A

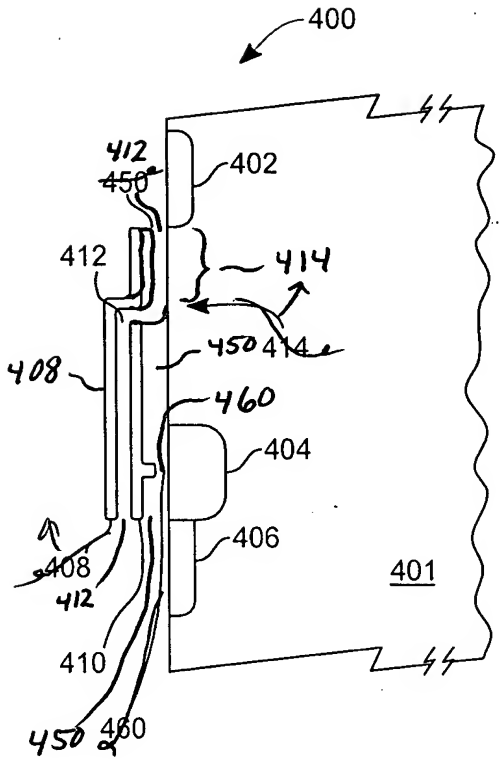

Fig. 4B